

REMARKS

Reconsideration of the application is respectfully requested for the following reasons:

1. In the Claims

The amendment to claim 1 has been submitted to improve the clarity of the subject matter for which protection is sought. The amendment was not made to avoid prior art, as it is believed that original claim 1 is fully patentable over the cited prior art. Rather, in reviewing the claim language it was perceived that some of the language could be improved to more clearly define the inventive subject matter. It is to be noted that the Examiner did not raise any objections with regard to the language of the original claims under 35 U.S.C. § 112 or any other part of the patent laws and regulations.

Applicant is grateful to the Examiner for indicating that claims 2-9 would be allowed if rewritten to include the limitations of claim 1. Applicant, however, has not rewritten claims 2-9 to include the limitations of claim 1 in view of the following comments regarding U.S. Patent 6,037,661 (Palagonia et al.) in relation to claim 1 of the present invention.

2. Rejection of claim 1 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 6,037,661 (Palagonia et al.)

Claim 1 stands rejected as being anticipated by Palagonia et al. For the reasons put forth below, Applicant respectfully traverses this rejection by asserting that Palagonia et al. does not disclose, suggest or teach the basic claimed memory chip module of claim 1.

a. Invention Described

According to claim 1, the present invention relates to a memory chip module including a first memory chip of a first type, a second memory chip of a second type

different from the first type of memory chip, and an electric connection between the first and second memory chips. The different types of memory chips are disposed one above the other in different levels and connected by vertical chip interconnections.

b. References Distinguished

Palagonia et al. discloses a multichip module including a first semiconductor chip mounted on top of a lead frame and a second semiconductor chip mounted and electrically coupled to the lead frame. Palagonia et al. appears to describe the multichip module as including at least one microprocessor (col. 2, lines 7-9; col. 2, lines 37-42).

As described above, claim 1 of the invention recites a "memory chip module" that includes first and second memory chips. Clearly, it is evident that Palagonia et al. does not disclose or suggest a "memory chip module" since Palagonia et al. describes at least one of the chips as being a "microprocessor." There is no description or teaching in Palagonia et al. of the chip module as comprising first and second memory chips. It follows that Palagonia et al. also does not describe that the chips are of two different types of memory chips and therefore, fails to teach every element of claim 1. Accordingly, Palagonia et al. does not describe, suggest or teach the memory chip module of claim 1 having two memory chips of different types.

In view of the above comments, Applicant submits that Palagonia et al. fails to anticipate the present invention recited in claim 1. Claims 2-9 are at least patentable due to their dependency from claim 1. Withdrawal of the rejection is respectfully requested.

3. Conclusion

In view of the foregoing remarks, it is respectfully submitted that the application is in condition for allowance. Accordingly, it is respectfully requested that claims 1-9 be allowed and the application be passed to issue.

Application No.: 09/926,791
Art Unit: 2818
Examiner: Michael T. TRAN

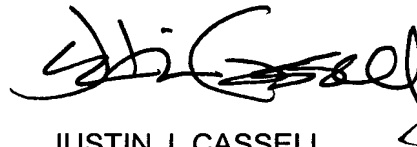
If any issues remain that may be resolved by a telephone or facsimile communication with the Applicants' Attorney, the Examiner is invited to contact the undersigned at the numbers shown below.

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Respectfully submitted,

A handwritten signature in black ink, appearing to read "Justin J. Cassell", with a long horizontal line extending to the right.

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